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10/562,869	04/07/2006	Walter Fix	411000-144	6418

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EXAMINER	
MONTALVO, EVA Y	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/562,869
Filing Date: April 07, 2006
Appellant(s): FIX ET AL.

William Squire
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 02/28/2011 appealing from the Final Office action mailed on 07/16/2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The Examiner is not aware of any pending appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 1, 3, and 8 are pending and rejected.

Claims 2 and 4-7 were previously canceled.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN

REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

4,494,108	**Clemen**	**01-1985**
6,429,450	**Mutsaers**	**08-2002**

NPL1, Wikipedia,"Equivalance series resistance", http://en.wikipedia.org/wiki/Equivalent_series_resistance, pp.1

NPL2, Wikipedia,"Capacitor", http://en.wikipedia.org/wiki/Capacitor, pp. 1

(9) Grounds of Rejection

Final Rejection

Specification

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. In the instant case, the description fails to provide support for "provide a potential at the gate electrode of the charging FET solely via the capacitive coupling", as it is recited in claim 1. Appropriate correction is required. See 37 CFR 1.75 (d) (1) and MPEP § 608.01(o).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it

pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1, 3 and 8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In the instant case, the limitation "provide a potential at the gate electrode of the charging FET solely via the capacitive coupling" in claim 1, is not disclosed in drawings or written descriptions.

4. The examiner notes that drawings and written description discloses a resistor 18 connected in parallel to the gate electrode of the charging FET and in between the capacitor 14 and the gate electrode. The resistor can also provide/affect a potential to the gate electrode depending on the current and resistance. Since the written description failed to disclose that the resistor does not provide any potential the gate electrode, the written descriptions and drawings does not support the limitation "provide a potential at the gate electrode of the charging FET solely via the capacitive coupling".

Remarks

5. Clemen in view of Mutsaers (cited in previous action) shows most limitations in the claims including a charging FET (5), a switching FET (2), and the drain/source electrodes of the charging and switching FET are connected in series, such that the gate of the charging FET is not connected directed to a voltage source, reference potential, input or output via an electrical line. The limitation in claim 1 of "provide a potential at the gate electrode of the charging FET solely via the capacitive coupling" is not disclosed by the prior art of record. However, said limitations

fails to satisfy the written description requirement under 35 U.S.C. 112, first paragraph, as set forth above in paragraphs 6 and 7. Claims 1-10 to would be allowable if the applicants overcomes the rejection under 35 U.S.C. 112, first paragraph by showing that there is sufficient written description to inform a skilled artisan that the applicants were in possession of the claimed invention as a whole at the time the application was filed. See MPEP § 2163 for guidelines pertaining the written description requirement.

(10) Response to Argument

Applicant argues:

The two grounds of the rejection are basically directed to the same issue, which is that there is no support for the claim 1 subject matter as follows and, in particular, the underlined portion, and thus this is new matter:

"wherein the gate electrode of the charging FET is directly capacitively coupled to one of the source/drain electrodes of the charging FET to thereby provide a potential at the gate electrode of the charging FET solely via the capacitive coupling" (underlining added)

Applicants submit this subject matter is not new matter, is permitted under the law and by the MPEP as discussed below as would be understood by one of ordinary skill. Patent applications and their claims are directed to those of ordinary skill in the electronics art who would have no problem in construing the present claim 1 as finding full support in the specification and would understand what is involved according to the filed specification.

The term "to dispense with a direct electrical coupling" means that in the embodiment with solely a capacitive coupling, the so called direct coupling may be eliminated, i.e., a resistive coupling. That is, there is only capacitive coupling intended by this section of the specification, if there is only capacitive coupling and not resistive coupling, then by definition there is solely only a capacitance involved in the circuit, which suggests that the resistances of Figs. 2 and 3, being optional, may be dispensed with. When the specification states that the resistances may be dispensed with, it is referring to Figs. 2 and 3, as would be understood by those of ordinary skill.

Examiner's reply:

Applicant's arguments are carefully considered but are not persuasive. The originally filed specification or drawings do not teach the claimed limitation "where the gate electrode of the charging FET is directly capacitively couple to one of the source/drain electrodes of the charging FET to thereby provide a potential at the gate electrodes of the charging FET solely via the capacitive coupling." (underline added) Although the specification teaches that the gate electrode of the charging FET is capacitively coupled to a source/drain electrode of the charging FET. This teaching does not exclude the gate electrode of the charging FET from being coupled to other elements in the circuit, to "thereby provide a potential at the gate electrode of the charging FET."

Furthermore, all capacitors have imperfections within the capacitor's material that create parasitic resistance (i.e., equivalent series resistance (ESR)), which means that a real capacitor can be modeled as a resistor connected in series with an ideal capacitor (see NPLs). An ideal capacitor would require specific materials that do not have any resistance. Applicant fails to disclose that the capacitor (i.e., formed by overlapping the gate electrode with source or drain electrode) is an idea capacitor nor that the electrodes (i.e., gate and source or drain) do not have any resistance (i.e., super conductors). Thus, unless otherwise clearly indicated, Applicant's disclosure does not teach the potential being provided at the gate electrode of the charging FET solely via the capacitive coupling.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Eva Yan Montalvo/
Examiner, Art Unit 2814

Conferees:

/Wael M Fahmy/

Supervisory Patent Examiner, Art Unit 2814

/Michael J Sherry/

Quality Assurance Specialist